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Low Power Optimization of Full Adder Using Modified XOR and XNOR Gates

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Abstract: *As proposed work, this work investigates the output of a Full Adder built using XOR/XNOR gates circuit designed with FET devices, specifically FinFET, in 32nm. The complete adder circuit is implemented using various logic types of XOR and XNOR layout, and it is compared to previous MOSFET-based circuits. Power Dissipation, Delay, and Power Delay are all terms used to describe how much power is dissipated, delayed, and HSPICE simulations are used to investigate the product of a complete adder, and waveforms are verified. The study seeks to determine which of the six exhibits the highest output with the least power consumption and propagation delay as opposed to their counterpart and proposed FinFET-based Full Adder Designs. As opposed to current circuits, these circuits are built to be faster and use less power. Because of the low output capacitance, this is probable. Each of the suggested complete adder circuits has its own set of advantages in terms of speed and power usage. Simulations for FinFETs in Shorted Gate Mode are performed using the HSPICE tool in 32-nm technology. In addition, the output of the proposed complete adder circuits is validated using waveforms produced by the Avanwaves Waveform generator.*

Keywords: FinFET, Short Gate Mode, Full Adder, XOR, XNOR, 32nm

I. INTRODUCTION

Universal electronic frameworks are an indistinguishable part of everyday life. Computerized circuitry, for example, microchips, sophisticated specialised gadgets, and advanced sign processors, make up a significant portion of electronic frameworks. If the scale of reconciliation grows, the convenience of circuits is limited by the power and zone consumption steps. As a result of the growing popularity and interest for battery-powered versatile devices, for example, mobile phones, tablets, and workstations, designers are attempting to reduce the resource consumption & territory of such frameworks while maintaining their speed. Increasing W/L ratio of semiconductors is one way to reduce power-delay result of circuit while avoiding problems caused by lowering stock voltage.

The widespread use of battery-powered portable electronic devices such as computers, tablets, notebooks, personal digital assistants, personal networking systems, among many others necessitates high efficiency circuits in terms of power consumption & processing speed in order to conserve electricity & process input data efficiently. Power use is omnipresent in VLSI systems. More heat is removed from a device as more fuel is dissipated. As a result, it not only reduces battery life but also necessitates a more powerful fan to keep device cool. As a result, power usage has a direct impact on a system's expense, weight, height, and battery life. In the other hand, in today's high-speed electronic applications, processing speed is critical. Power consumption is a limiting factor in increasing clock rate & circuit density. Many VLSI implementations rely heavily on arithmetic operations, such as, image, digital signal processing & video processing, microcontrollers, microprocessors. The most common arithmetic operations are addition, subtraction, multiplication, and multiply and aggregate. The extension feature could be used to perform any of the above operations. As a result, a 1-bit complete adder cell continues to play a crucial role in deciding overall device efficiency metrics. A 1-bit complete adder cell is also used in a floating-point uni, processor's arithmetic logic array & address generation for cache or memory entry. Until now, several complete adder cells with various logic types have been published in the literature using metal–oxide–semiconductor FET (MOSFET) technology, each with its own set of advantages & disadvantages.

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The number of transistors per square inch of an integrated circuit would virtually double every 18 months Moore projected in 1965. This rule means that silicon bulk transistors (i.e., MOSFETs) should be constantly scaled down. Transistors' measurements have historically been shrunk down, to the point that they currently exist in the nanometre range. There are several problems that prevent MOSFETs from dwindling any more. Nanometre silicon bulk transistors, for example, face new challenges such as drain-induced barrier lowering, short channel effects reduced gate controllability, hot electron effect, & so on. As a consequence, there is a strong incentive to create new devices such as the carbon nanotube field effect transistor, single electron transistor, FinFET, & so on.

II. IMPLEMENTATION

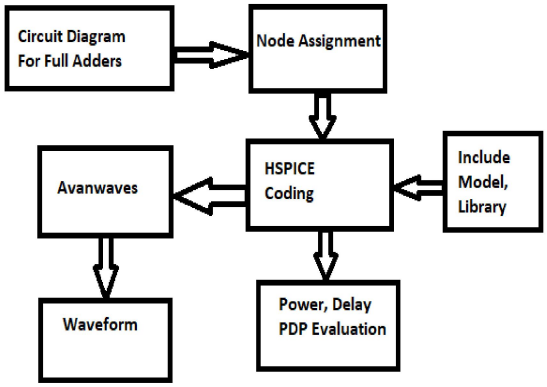

Figure 1: Methodology

In this section, methodology of the implementation is explained. While implementing in VLSI back end on Synopsys HSPICE Software, there is requirement to make circuit diagram with node numbers. After adding the node numbers, an HSPICE netlist is written and then simulated, several parameters like input/output waveforms are studied. Also, calculation of power, delay and other parameters are done. All these steps are repeated for all circuits. The technology node methodology used is 32nm for FinFET. This constitutes the implementation of full adder.

The implemented circuits are shown in figure 3 and the internal XOR/XNOR circuits are shown in figure 2. the circuit working is verified under HSPICE and its authenticity is validated by reference paper [1].

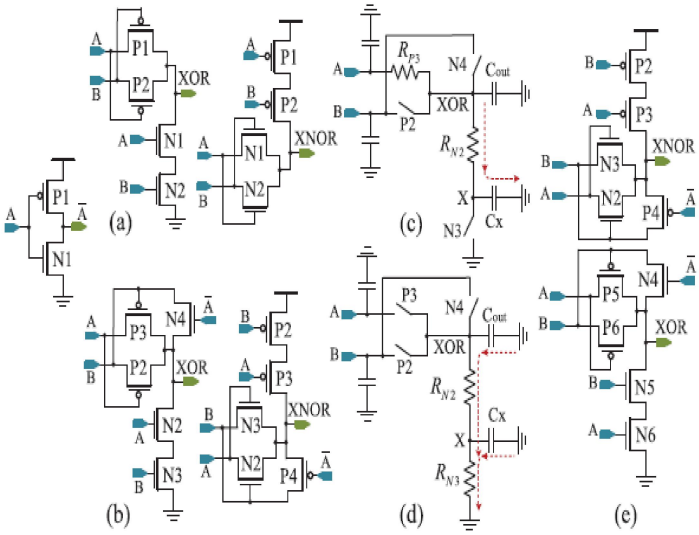

Figure 2: XOR/XNOR circuits to be used in Full Adder [1]

The adders are basically made using the above XOR/XNOR circuits which are made in different configurations such as Non full swing configuration and full swing configuration which was proposed earlier in [1]. The figure c and d are the RC model configuration of the same circuit and e is the final XOR/XNOR circuit which is used in making of the full adders.

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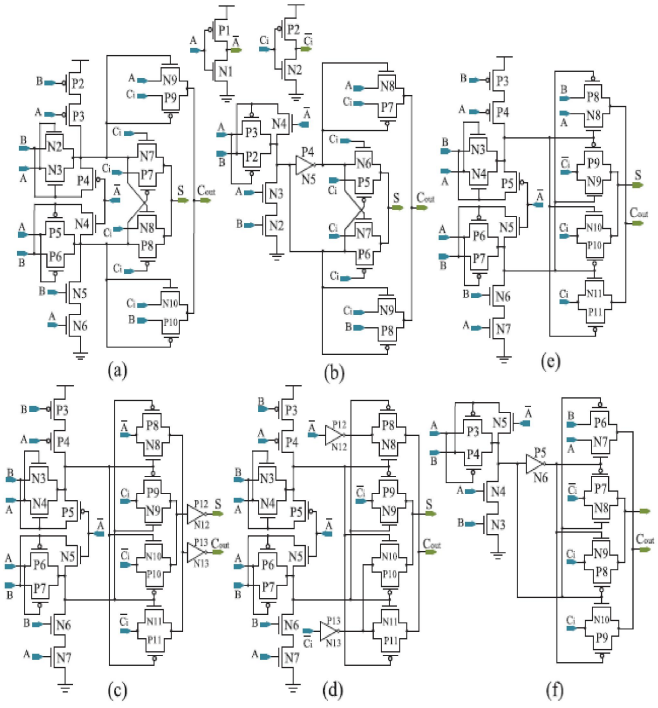

Figure 3: Full Adder Circuits using XOR/XNOR

The e figure in Figure 2 is used in all the above Full Adder circuits which are basically the different configuration of the adder as per the number of transistor count.

The proposed work is done on FinFET by using it in shorted gate mode for circuit b and circuit f mentioned in previous section as its performance is best under the parametric results. The implemented circuit using FinFET is shown below for Circuit b.

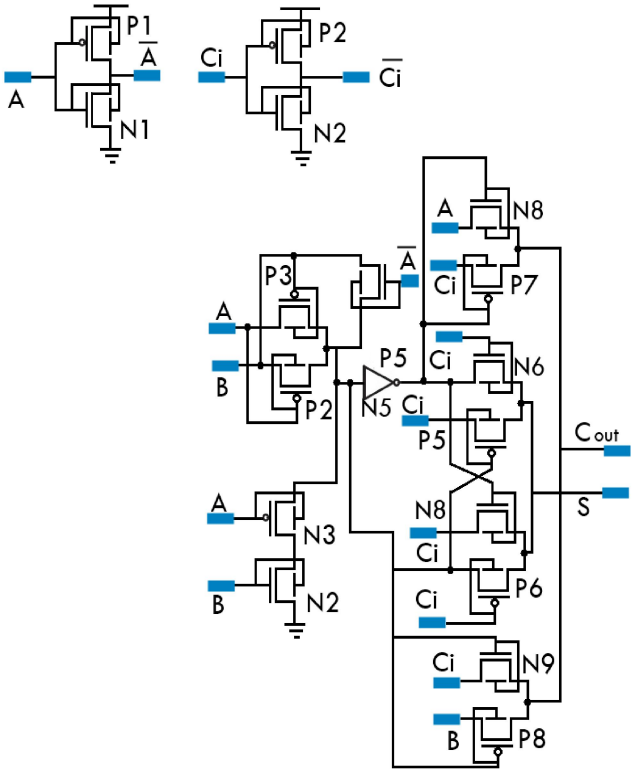

Figure 4: Full Adder Circuit b using FinFET (proposed)

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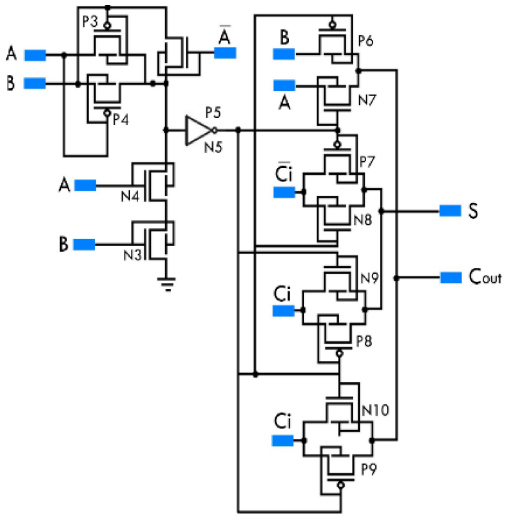

Figure 5: Full Adder Circuit f using FinFET (proposed)

In the above figure 5 the full adder circuit for Circuit f using FinFET is given which is the final proposed circuit for the full adder.

II. RESULT

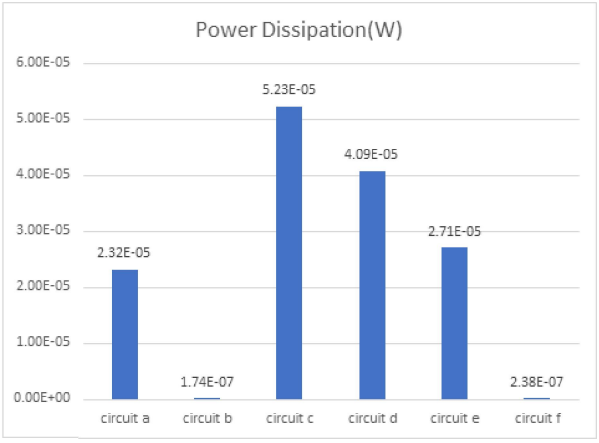

Figure 6: Power Result (MOSFET)

In figure 6 to 8, the results for MOSFET based six circuits are shown. Out of which circuit b and circuit f perform best and hence they are considered for proposed circuits.

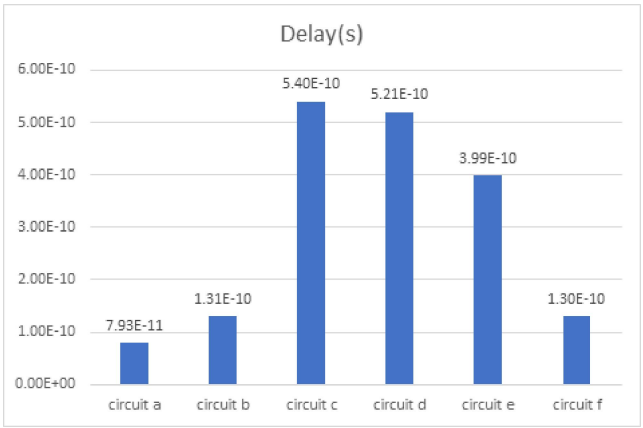

Figure 7: Delay Result (MOSFET)

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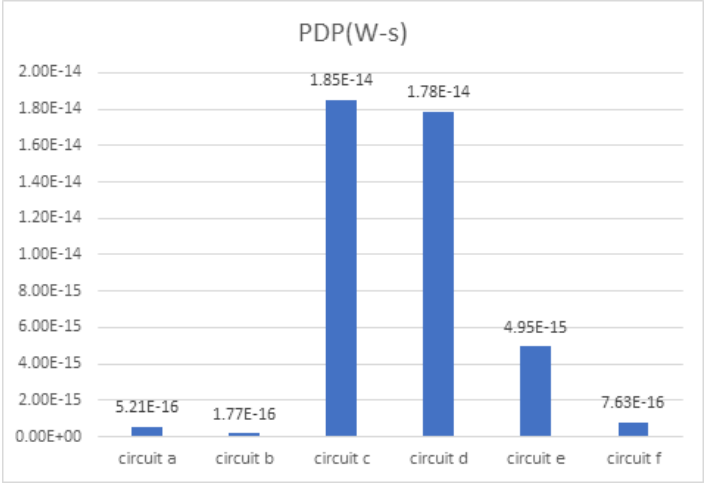

Figure 8: PDP Result (MOSFET)

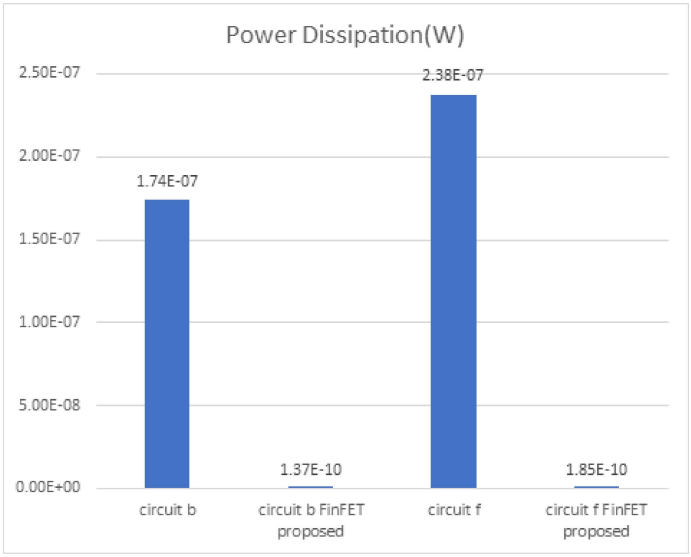

Figure 9: Power Result

In figure 9 to 11, the circuit b and circuit f proposed are compared with counterpart and show that they perform better in all circumstances.

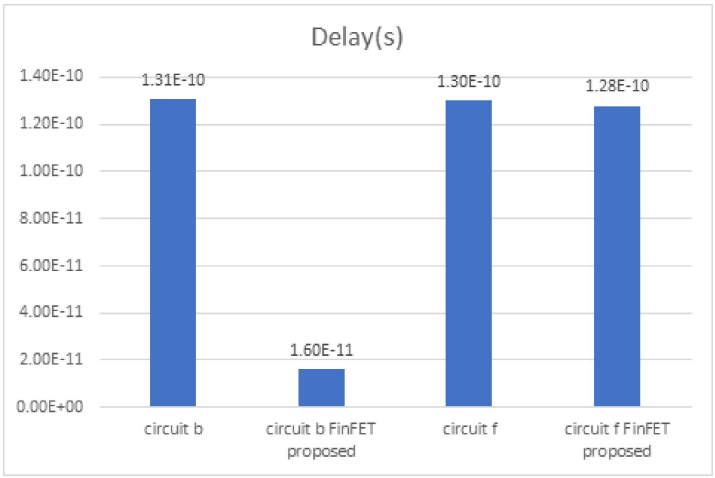

Figure 10: Delay Result

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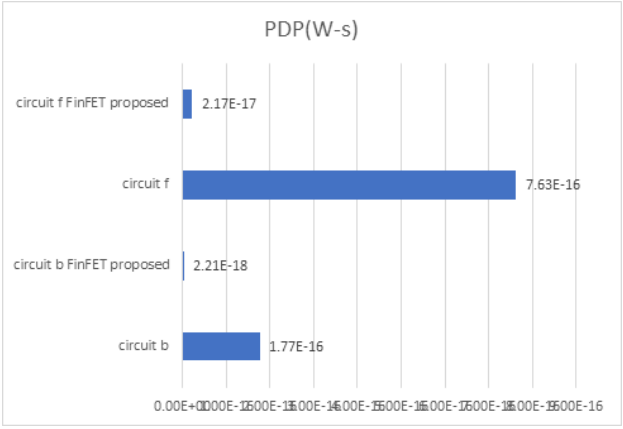

Figure 11: PDP Result

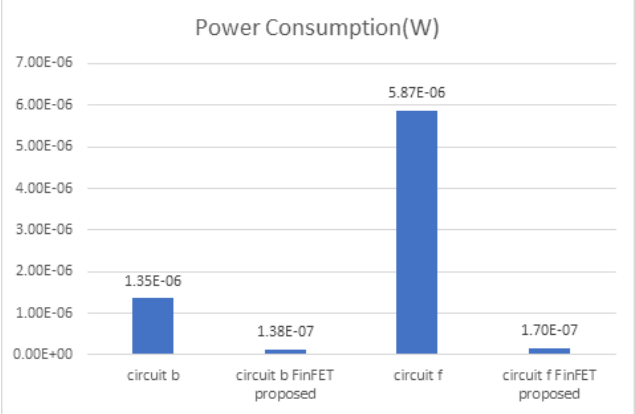

Figure 12: Power Consumption Result

III. Conclusion

The presented design is simulated using FinFET of BSIM-CMG model and HSPICE software. HSPICE is the software for SPICE simulation from Synopsys. The reason to use this software is compatibility of libraries of FinFET. In literature over the years Since a complete adder is so important in deciding the output parameters of an entire digital device, several prototypes have been discussed. In terms of power consumption and speed, each of these designs has advantages and disadvantages. A complete adder may be classified as either dynamic or static. While a dynamic style full adder has a smaller on-chip area & faster operation than a static style full adder, it has some inherent disadvantages such as charge sharing, heavy clock load, poor noise immunity & leakage. Finally, the proposed circuit using FinFET technology improves the power, PDP, and delay in both circuits.

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